



CBM3082 Datasheet

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Revision History

Date	Rev No	Description
2008-10-29	1.0	Initial release
2009-1-14	1.1	Update QFN package

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1 Description

Most flexible SD/MMC memory card Controller with dedicated 32-bit microprocessor

The CBM3082 is the most flexible SD/MMC memory card controller on the market. The proprietary 32 bit processor was specially tailored to handle both SD/MMC protocol and Flash access. Software change can be made easily on site to support new flash or solve potential compatibility issue.

CBM3082 support SD2.0 and MMC 4.2 standard. Which are backward compatible to the earlier SD/MMC version, such as SD1.0, SD1.01, SD1.1, and MMC 3.31, MMC4.0, MMC4.1 etc. Up to speed class 6 can be achieved with certain Flash type. CPRM is supported for SD card. It also supports sleep mode, which can cut down power consumption significantly.

With dual-channel mode enabled, CBM3082 can reach theoretical flash access speed limit of 24MByte/s for read and 16MByte/s for write. The on-the-fly ECC engine is capable of correcting and detecting up to 8bit errors per 528bytes page. For data security, CBM3082 is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

The CBM3082 supports all NAND/MLC flash memory available in the market. New flash can be supported by software re-configuration. Card with capacity up to 32GB can be made when configured as SDHC card. Card with capacity up to 128GB can be made when configured as MMCHC card.

The CBM3082 runs smoothly with various hosts. Substantial tests have been made to make sure the compatibility with different hosts.

The CBM3082 is available in 48-pin TQFP and 48-pin QFN package, which are thinnest and smallest on the market. The 48-pin CBM3082 supports up to 4 flash chips. Customers can choose different packages to meet their design requirement.

2 Features

■ **SD card standard**

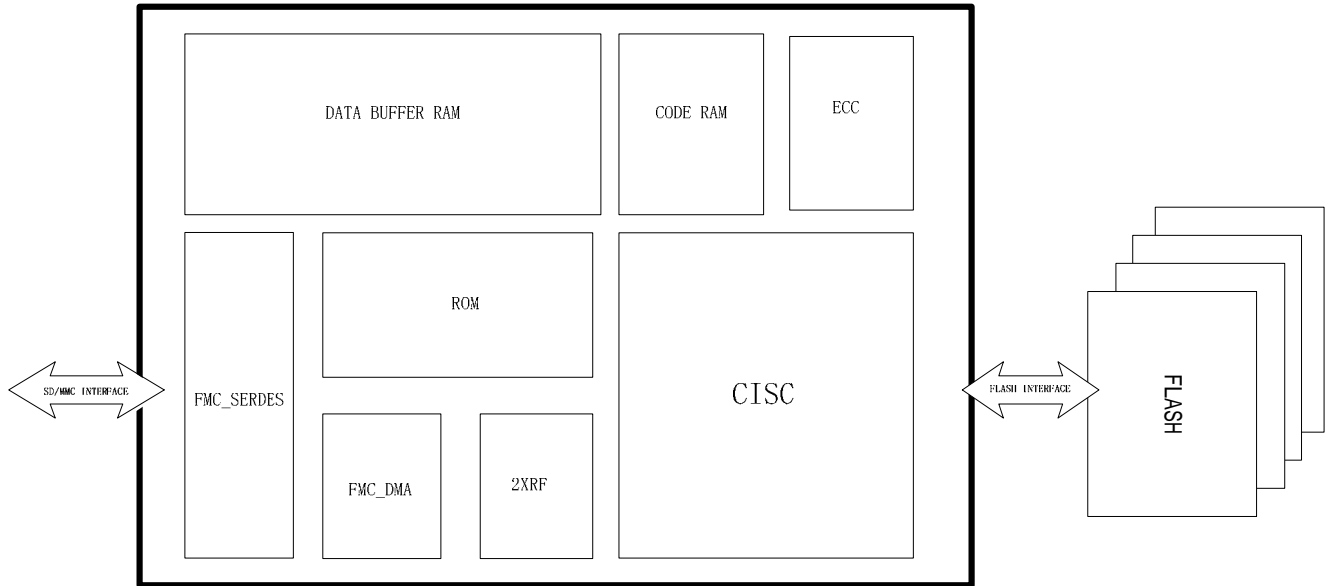
- System specification SD2.0 compliance.
- SPI mode supported
- Command class 0,2,4,5,6,7,8,10 supported
- CPRM supported
- Speed class up to 6
- Support host clock up to 50 MHz
- Supported bus width: X1, X4
- Supported sleep mode

■ **MMC card standard**

- System specification MMC4.2 compliance.
- SPI mode supported
- Command class 0 to 8 supported
- Support host clock up to 52 MHz
- Supported bus width: X1, X4, X8
- Dual voltage MMC supported
- Supported sleep mode

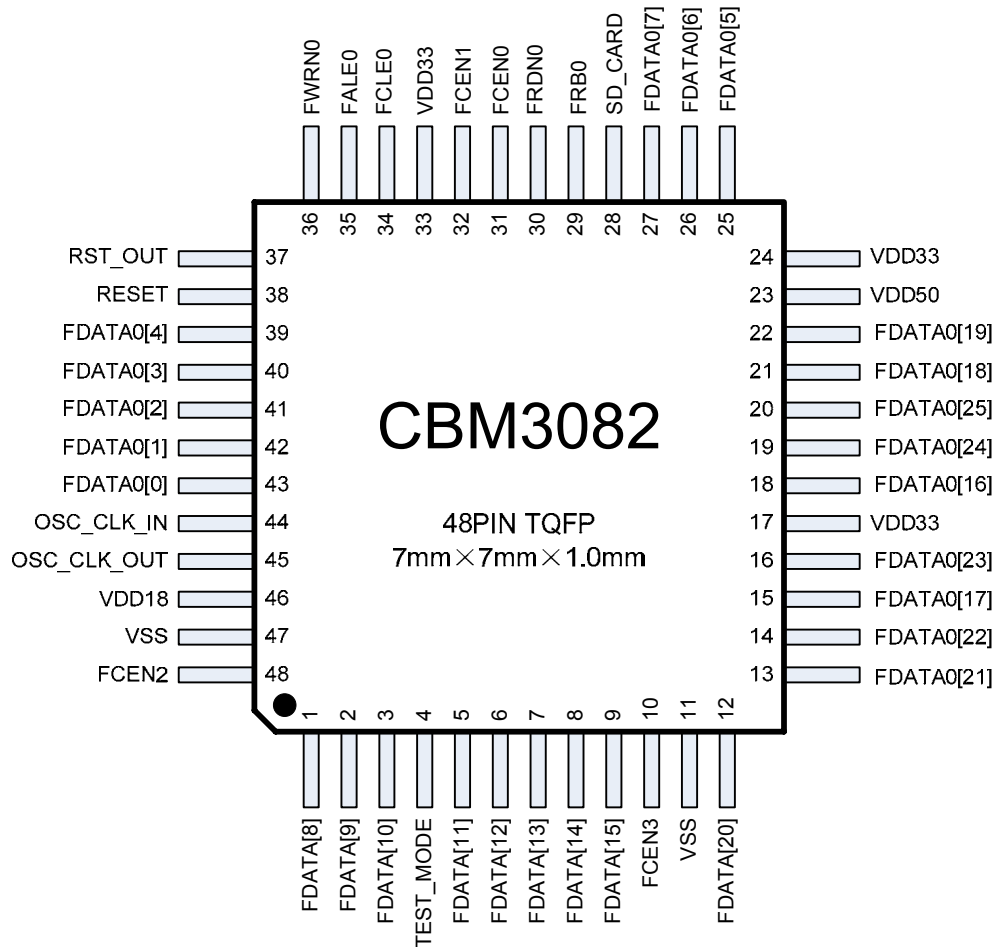
- **Fastest data transfer rate on the market :**
Single-channel mode: 18MB/s for Read, 15MB/s for Write
- **On-the-fly ECC built-in Hardware enhances reliability**
ECC for Binary NAND flash: 8 bit/page (1 page = 528 bytes)
ECC for MLC NAND flash: 8 bit/page
- **Hardware & Software Data Protection Technology**
Prevent data corruption even if it is powered off or unplugged during data transfer.
- **NAND& MLC Flash Interface**
Supports Samsung & Toshiba NAND flash memories
Supports Toshiba & Sandisk MLC flash memories
Supports Infineon / Hynix flash memories
Supports ST Microelectronics flash memories
Supports Micron / Actrans flash memories
Software configuration to support various new flash memories
Supports up to 8 flash chips.
- **Proprietary 32-bit CISC microprocessor feature**
Proprietary 32-bit CISC processor for SD/MMC protocol processing and flash access.
Single cycle instruction period
- **Low power dissipation**
R/W Operating current 34.6 mA
- **Leading 0.18um CMOS technology**
- **48-pin TQFP or QFN package**
48-pin CBM3082 supports up to 4 Flash Chips

3 Block Diagram



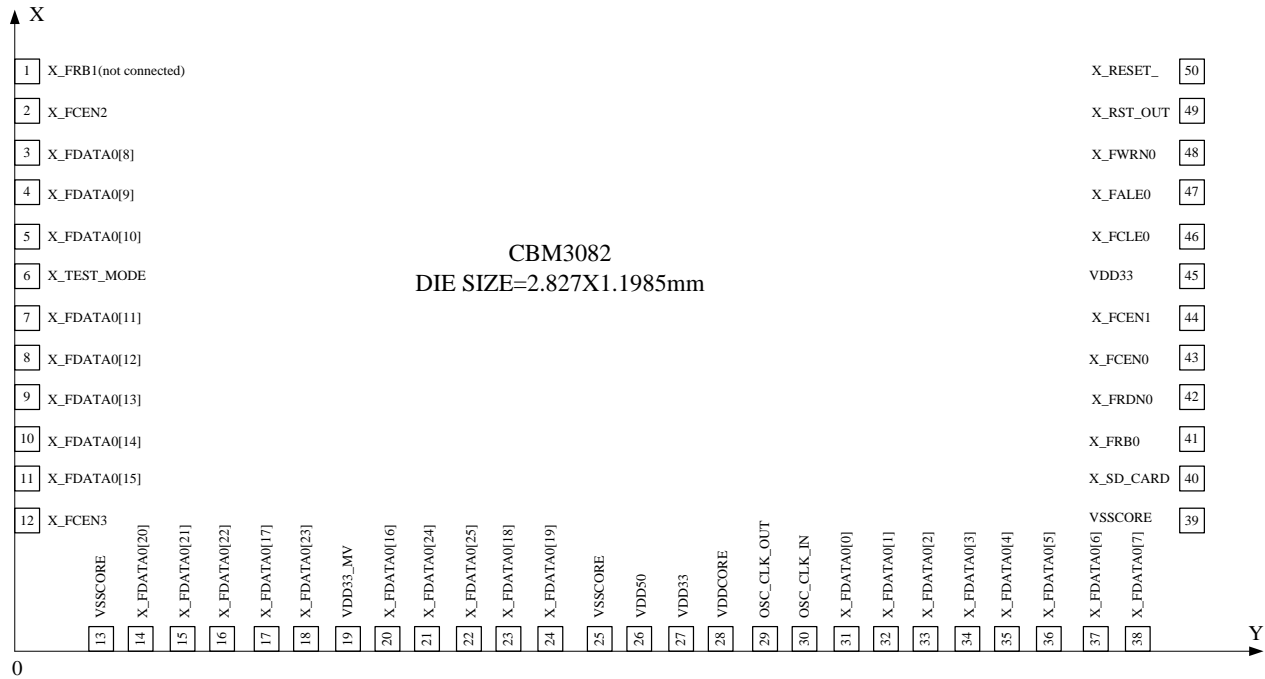
4 Pin Assignment

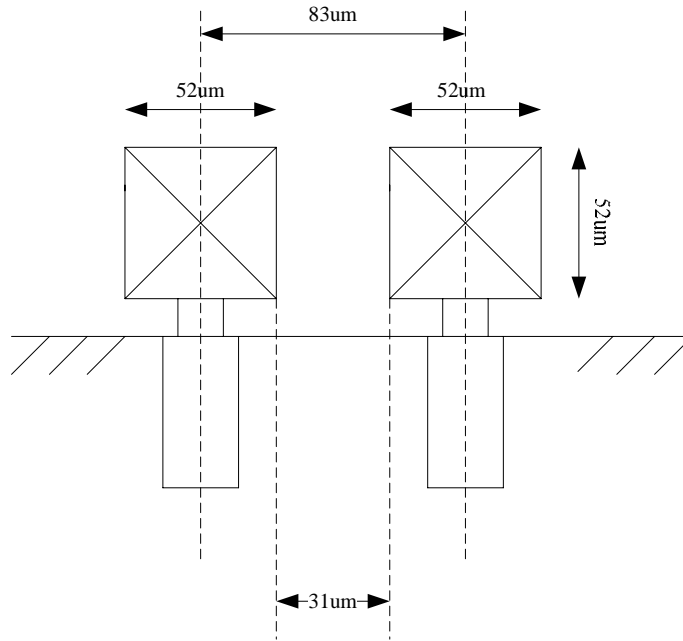
4.1 TQFP48 (Top Side)



4.2 QFN48 (Top Side)

4.3 Die Outline (Top View)





CBM3082 minimum pad size is 52 um x 52 um, minimum pad pitch is 83 um

5 Pin Description

Brief CBM3082 pin functions are shown in the following tables.

- I** : Input signal
- O** : Output signal
- I/O** : Bi-direction signal
- PWR** : Power signal
- GND**: Ground signal

CBM3082 TQFP48 / QFN48 Pin Description

CBM3082 TQFP48 Pin No.	CBM3082 QFN48 Pin No.	Pin Name	Type	Description
11	1	VSS	GND	Ground
12	2	FDATA0[20]	I/O	Data Bus - bit 20
13	3	FDATA0[21]	I/O	Data Bus - bit 21
14	4	FDATA0[22]	I/O	Data Bus - bit 22
15	5	FDATA0[17]	I/O	Data Bus - bit 17
16	6	FDATA0[23]	I/O	Data Bus - bit 23
17	7	VDD33	PWR	3.3V Power
18	8	FDATA0[16]	I/O	Data Bus - bit 16
22	9	FDATA0[19]	I/O	Data Bus - bit 19
45	10	OSC_CLK_OUT	O	Crystal Output
44	11	OSC_CLK_IN	I	Crystal Input
40	12	FDATA0[3]	I/O	Flash Data Bus - bit 3
39	13	FDATA0[4]	I/O	Flash Data Bus - bit 4
25	14	FDATA0[5]	I/O	Flash Data Bus - bit 5
26	15	FDATA0[6]	I/O	Flash Data Bus - bit 6
27	16	FDATA0[7]	I/O	Flash Data Bus - bit 7
47	17	VSS	GND	Ground

28	18	SD_CARD		
29	19	FRB0	I	Group Flash Ready_Busy
30	20	FRDN0	O	Group Flash Read Enable (active low)
31	21	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
32	22	FCEN1	O	Flash Chip Enable - Chip 1 (active low)
33	23	VDD33	PWR	Pad ring 3.3V Power
34	24	FCLE0	O	Group Flash Command Latch Enable
35	25	FALE0	O	Group Flash Address Latch Enable
36	26	FWRNO	O	Group Flash Write Enable (active low)
37	27	RST_OUT	O	Chip reset output/ External device reset signal
38	28	RESET	I	Reset Sign (active low)
41	29	FDATA0[2]	I/O	Flash Data Bus - bit 2
42	30	FDATA0[1]	I/O	Flash Data Bus - bit 1
43	31	FDATA0[0]	I/O	Flash Data Bus - bit 0
46	32	VDD18	PWR	Regulator 1.8V Out
24	33	VDD33	PWR	Regulator 3.3V Power OUT
23	34	VDD50	PWR	Regulator5V Power Input
21	35	FDATA0[18]	I/O	Data Bus - bit 18
20	36	FDATA0[25]	I/O	Data Bus - bit 25
19	37	FDATA0[24]	I/O	Data Bus - bit 24
48	38	FCEN2	O	Flash Chip Enable - Chip 2 (active low)
1	39	FDATA0[8]	I/O	Flash Data Bus - bit 8
2	40	FDATA0[9]	I/O	Flash Data Bus - bit 9
3	41	FDATA0[10]	I/O	Flash Data Bus - bit 10
4	42	TEST_MODE	I	Test Mode Enable Pin
5	43	FDATA0[11]	I/O	Flash Data Bus - bit 11

6	44	FDATA0[12]	I/O	Flash Data Bus - bit 12
7	45	FDATA0[13]	I/O	Flash Data Bus - bit 13
8	46	FDATA0[14]	I/O	Flash Data Bus - bit 14
9	47	FDATA0[15]	I/O	Flash Data Bus - bit 15
10	48	FCEN3	O	Flash Chip Enable - Chip 3 (active low)

All 26 FDATA0 pins can be used as bidirectional GPIOs. Among these pins, FDATA0[16] to FDATA0[25] are normally used as SD/MMC interface pins. FDATA0[0] to FDATA0[15] are used as two flash data channels. If only 1 flash data channel (FDATA0[0] to FDATA0[7]) is used, the other channel can be used for other purpose. Each of the GPIO pins can be controlled separately.

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions		min	max	unit
VDD50	supply voltage			-0.5	4.5	v
VI	input voltage			-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A	SD/MMC pins	-4000	+4000	v
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k Ω resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VDD50	digital supply voltage		3.0	3.3	3.6	V
VI	input voltage		0	-	VDD50	V
Tamb	ambient temperature		0	-	+70	

6.3 Static characteristics

All parameters are measured at VDD50 = 3.0 to 3.6 V; VSS = 0 V; Tamb = 40 to 85 ;

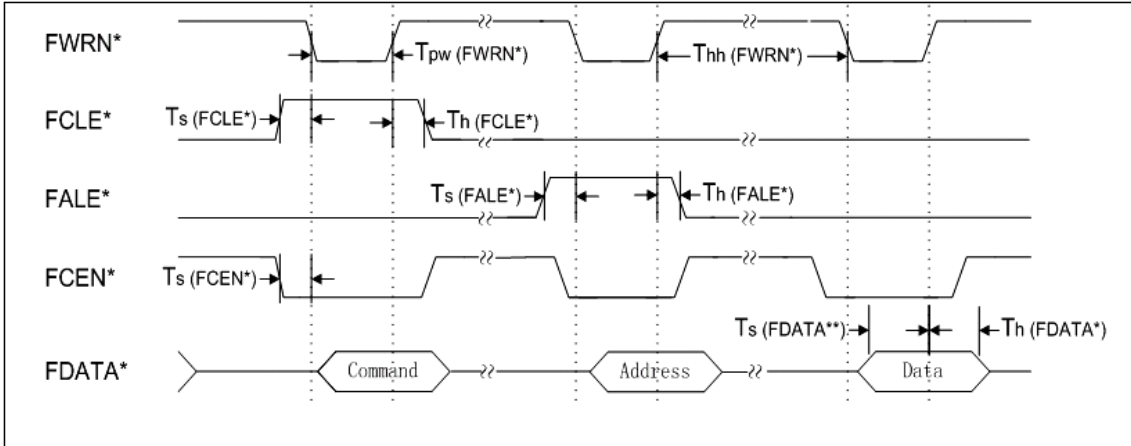
symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	R/W operating supply current	R/W operational mode		34.6		mA

6.4 Dynamic characteristics

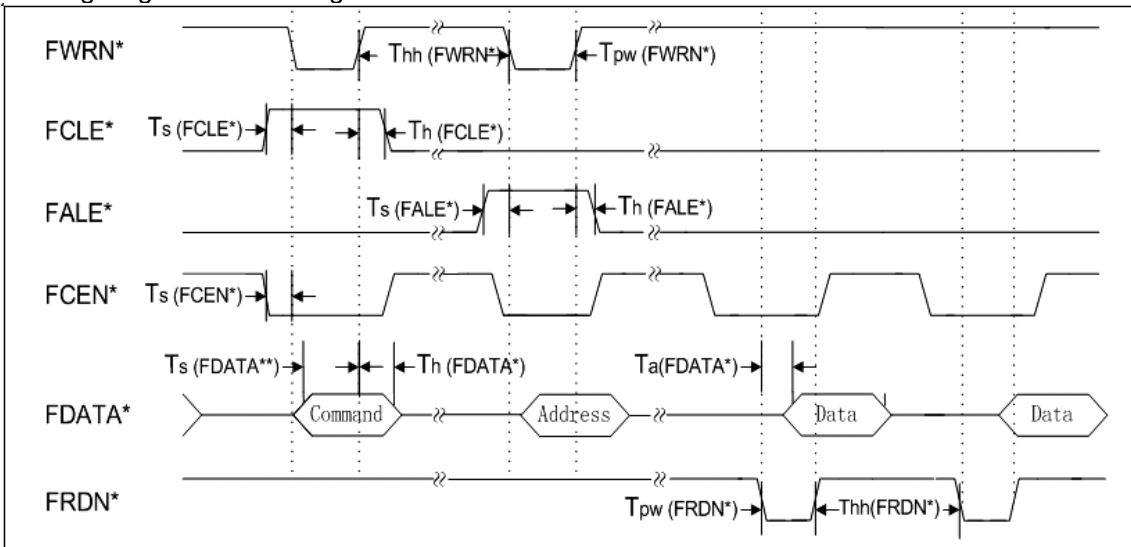
All parameters are measured at VDD50 = 3.0 to 3.6 V; VSS = 0 V; Tamb = 40 to 85 ;

symbol	Parameter	conditions	min	Typ	max	Unit
Ts(FDATA*)	FDATA* setup time relative to rising FWRN* edge		-	33	-	ns
Th(FDATA*)	FDATA* hold time relative to falling FWRN* edge		-	33	-	ns
Ts (FCLE*)	FCLE* setup time relative to falling FWRN* edge		-	33	-	ns
Th (FCLE*)	FCLE* hold time relative to rising FWRN* edge		-	33	-	ns
Ts (FALE*)	FALE* setup time relative to falling FWRN* edge		-	33	-	ns
Th (FALE*)	FALE* hold time relative to rising FWRN* edge		-	33	-	ns
Ts (FCEN*)	FCEN* setup time relative to falling FWRN* edge		-	99	-	ns
Tpw (FWRN*)	FWRN* Pulse Width		-	33	-	ns
Thh (FWRN*)	FWRN* high hold time		-	33	-	ns
Ta(FDATA*)	FDATA* access time relative to falling FRDN* edge		-	-	40	ns
Tpw (FRDN*)	FWRN* Pulse Width		-	33	-	ns
Thh (FRDN*)	FWRN* high hold time		-	33	-	ns

Timing diagram for Writing of Data

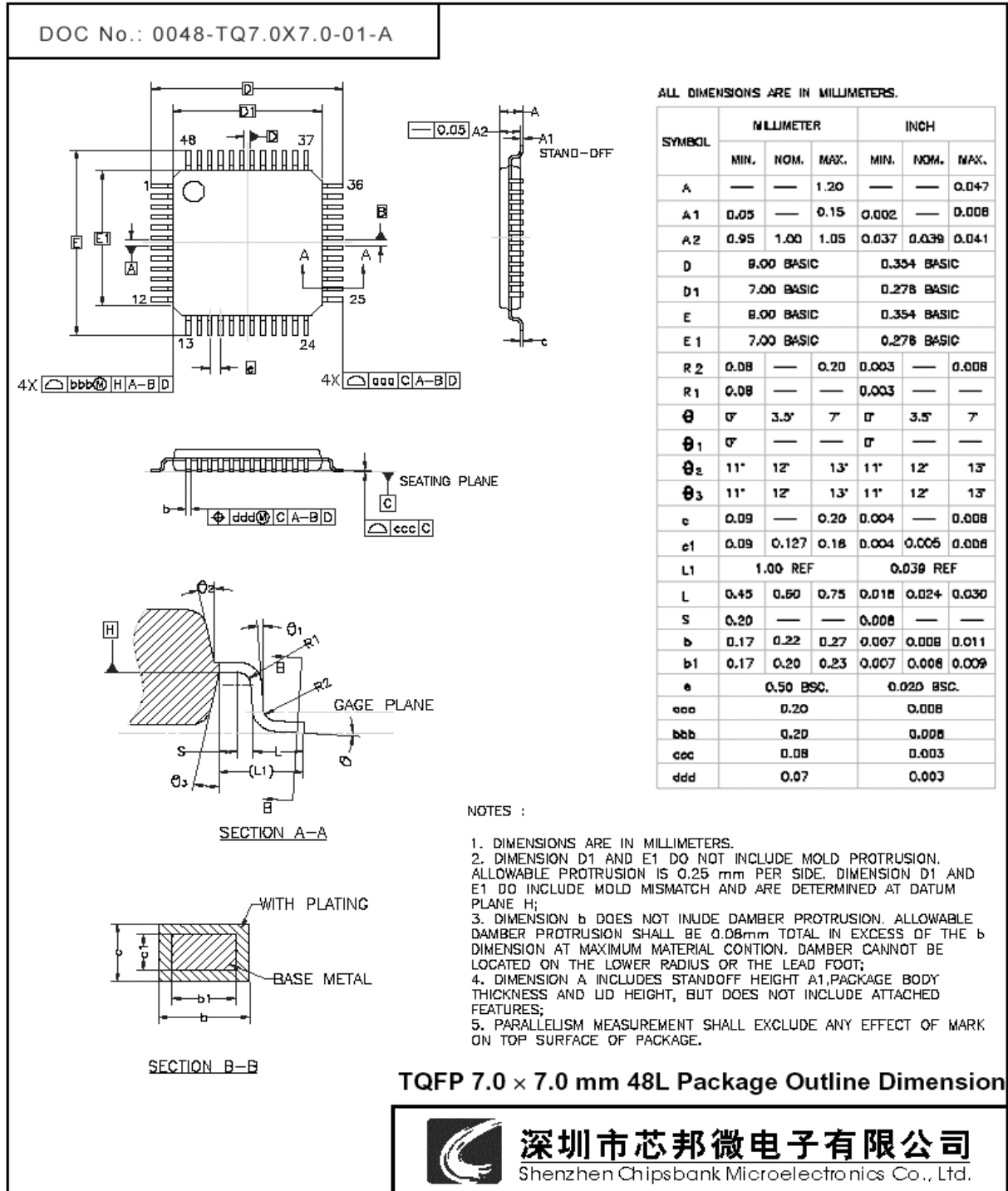


Timing diagram for Reading of Data



7 Mechanical Dimensions

7.1 48-Pin CBM3082 TQFP Package Outline Dimension



7.2 48-Pin CBM3082 QFN Package Outline Dimension

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